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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
| 10/583,525 | 06/16/2006 | Andrew Holland | 1662-2 PCT/US | 8381 |
| 23869 | 7590 | 02/17/2010 | EXAMINER | |
| HOFFMANN & BARON, LLP 6900 JERICHO TURNPIKE SYOSSET, NY 11791 | | | TRAN, THIEN F | |
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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| Office Action Summary | Application No. 10/583,525 | Applicant(s) HOLLAND, ANDREW |
| | Examiner Thien F. Tran | Art Unit 2895 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If no period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 30 November 2009.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1,3-20,23,24 and 43-50 is/are pending in the application.
 - 4a) Of the above claim(s) 6,9-19 and 23 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1,3-5,7,8,20,24,43-50 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) Notice of Informal Patent Application
- 6) Other: _____

DETAILED ACTION

Claim Objections

Claim 1 is objected to because of the following informalities: line 6, "a heat radiating portion" should be "a heat radiating surface". Appropriate correction is required.

Claim 3 is objected to because of the following informalities: line 3, "a printed circuit board facing said surface" should be "a printed circuit board facing surface". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 3-5, 7-8, 20, 24, 43-50 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recitation of "a plurality of semiconductor dies" and "one or more second chips" in claim 1 sets forth structure not supported by the elected embodiment of Fig. 2. The elected Fig. 2 shows one chip and one die. Applicant is requested to explain and point out which element in the elected Fig. 2 is considered as a second die and a second chip.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-5, 8, 20, 47-50, insofar as in compliance with 35 USC 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Sakanobu et al. (JP 07-288332).

Sakanobu et al. discloses a mounted semiconductor assembly comprising: a semiconductor assembly consisting of a single semiconductor die consisting of a first chip (12) stacked or flip-mounted thereon; a first portion (21-6) for mounting the semiconductor assembly; a second portion (21-5) inherently having a heat radiating surface; and a connecting portion (portion 21 between lines E and F) joining the first and second portions and arranged to allow folding of the second portion over the first portion to form a cover (see Fig. 7), wherein the mounting comprises a sealing material (14', 24) at least partially encapsulating the mounting and the semiconductor assembly such that at least part of a printed circuit board facing surface of the first portion and/or the heat radiating surface of the second portion are left exposed.

Regarding claim 3, the first portion of the mounting comprises a formation of electrical connectors (21-1 to 21-4), each of which has a printed circuit board facing surface, which is not covered by the sealing material.

Regarding claim 4, the second portion is arranged to be in a spaced parallel relationship with the first portion.

Regarding claim 5, the second portion further comprises at least one additional edge portion arranged to extend when the mounting is folded beyond at least one edge of the first portion of the mounting (Fig. 7-2).

Regarding claim 8, the connecting portion is provided with folding means to enable the folding of the second portion over the first portion (Fig. 7-2).

Regarding claim 20, the formation of electrical connectors (21-1 to 21-4) is in spaced relationship with the first portion (21-6) and are linked electrically with the semiconductor assembly (12) via connectors (21-4, 21-7).

Regarding claim 47, the second portion is continuous.

Regarding claim 48, the second portion is inherently functioning as a heatsink.

Regarding claim 49, the second portion (shielding piece) is inherently functioning as a low resistance and low inductive path to ground (see claim 1).

Regarding claim 50, the second portion is capable of functioning as local electromagnetic shield.

Note that the functional languages in claims 48, 49 and 50 are taken as inherent of the structure otherwise claimed rather than additional structural limitations.

Claims 1, 3-5, 7-8, 20, 24, 43, 47-50, insofar as in compliance with 35 USC 112, are rejected under 35 U.S.C. 102(b) as being anticipated by Sakanobu et al. (JP 07-288332).

Kazuo et al. discloses a mounted semiconductor assembly comprising: a semiconductor assembly consisting of a single semiconductor die consisting of a first chip (15) stacked or flip-mounted thereon; a first portion (7) for mounting the

semiconductor assembly; a second portion (8, 9) having a heat radiating surface; and a connecting portion (10) joining the first and second portions and arranged to allow folding of the second portion over the first portion to form a cover, wherein the mounting comprises a sealing material (40) at least partially encapsulating the mounting and the semiconductor assembly such that at least part of a printed circuit board facing surface of the first portion and/or the heat radiating surface of the second portion are left exposed.

Regarding claim 3, the first portion of the mounting comprises a formation of electrical connectors (6b), each of which has a printed circuit board facing surface, which is not covered by the sealing material.

Regarding claim 4, the second portion (8, 9) is arranged to be in a spaced parallel relationship with the first portion.

Regarding claim 5, the second portion (8, 9) further comprises at least one additional edge portion arranged to extend when the mounting is folded beyond at least one edge of the first portion (tab 7) of the mounting.

Regarding claim 7, Kazuo et al. also discloses the mounting is formed from a single sheet (1) of electrically and thermally conducting material (leadframe 1 in Fig. 2).

Regarding claim 8, the connecting portion is provided with folding means to enable the folding of the second portion over the first portion (Figs. 11-12).

Regarding claim 20, the formation of electrical connectors (6b) is in spaced relationship with the first portion (7) and are linked electrically with the semiconductor assembly (15).

Regarding claim 24, the mounting is part of an array of a plurality of mountings (two or more unit leadframes 2, Fig. 7).

Regarding claim 43, the single sheet (1) of electrically and thermally conducting material is copper.

Regarding claim 47, the second portion (8, 9) is continuous.

Regarding claim 48, the second portion is functioning as a heatsink.

Regarding claim 49, the second portion is capable of functioning as a low resistance and low inductive path to ground.

Regarding claim 50, the second portion is a copper cover that is capable of functioning as a local electromagnetic shield.

The claim limitations “functioning as a heatsink” in claim 48, “functioning as a low resistance and low inductive path to ground” in claim 49, and “functioning as a local electromagnetic shield” in claim 50 are functional languages and are nonlimiting since it has been held that claims directed to apparatus must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). “Apparatus claims cover what a device is, not what a device does.” Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990). A claim containing a “recitation with respect to the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus” if the prior art apparatus teaches all the structural limitations of the claim. Ex parte Masham, 2 USPQ2d 1647 (Bd. Pat. App. & Inter. 1987).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7, 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakanobu et al. (JP 07-288332) in view of Kierse (US 5,541,446).

Sakanobu et al. also discloses the mounting is formed from a same conducting material (leadframe 21). Sakanobu et al. does not disclose that the leadframe (21) is copper. Kierse discloses a leadframe made of copper. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to form the leadframe of Sakanobu of copper in order to improve heat dissipation. Copper is an electrically and thermally conducting material.

Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakanobu et al. (JP 07-288332).

Sakanobu does not disclose the mounting is part of an array of a plurality of mountings. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a plurality of mountings, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. St. Regis Paper Co. v. Bemis Co., 193 USPQ 8.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

Art Unit: 2895

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37

CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F. Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 7:30AM - 4:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew N. Richards can be reached on (571) 272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

Art Unit: 2895

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Thien F Tran
Primary Examiner
Art Unit 2895

/Thien F Tran/
Primary Examiner, Art Unit 2895